| No | Course Information (2019-2020) | |
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| 1 | Unit name: | Digital Design with HDL |
| 2 | Code: | EcE 41021 |
| 3 | Classification: | Engineering subject |
| 4 | Credit value: | 3 |
| 5 | Semester/ Year Offered: | 1/4 |
| 6 | Pre-requisite: | EcE 21021 & 22021 Digital Electronic<br>EcE 21014 & 22014 Technical Programming |
| 7 | Mode of delivery: | Presentation, computer application |
| 8 | Assessment system and breakdown of marks: | Tutorial, Lab report |
| | Assignment / Tutorial | 10% |
| | Lab Report | 20 % |
| | Exam Q & A | 70% |
| 9 | Academic staff teaching unit: | Department of Electronic Engineering |
| 10 | Course outcome of unit:<br>After completion of this course, students will be able to<br>1. Describe the configuration of logic circuits, the design process for digital hardware implementation and implementation technology for CPLD and FPGA<br>2. Examine the various logic circuit problems and the number representation problems (by applying the Boolean Algebra, Karnaugh Map and signed number and unsigned number representation)<br>3. Design the digital circuits by using logic gates or blocks or VHDL code<br>4. Investigate VHDL code and operations of digital circuits using Quartus II software and DE2-115 FPGA Board and analyze the results with the digital waveforms | |
| 11 | Synopsis of unit:<br>This course provides a systematic introduction to the topic of VHDL programming for designing embedded digital system .It emphasizes the basic ideas of design concepts of digital hardware and the practical aspects of implementing technology for CPLD and FPGA devices. It also presents the optimized implementation of logic circuit, arithmetic circuit and combinational circuit, synchronize and asynchronize circuit using VHDL code. Digital systems are also designed by using building blocks and clock synchronization. In addition , this course includes the data flow Design Concepts, Introduction to Logic | |

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| | Circuit, Implementation Technology, Optimized Implementation of Logic Function, Number Representation and Arithmetic Circuits, Combinational – Circuit Building Blocks, Flip-Flops, Registers, Counters, Simple Processors, Synchronous and Asynchronous Sequential Circuits and Digital System Design. |
| 12 | Topic:<br>**Chapter 1 Design Concepts**<br>1.1 Digital Hardware<br>1.2 The Design Process<br>1.3 Design of Digital Hardware<br>1.4 Logic Circuit Design in This Book<br>1.5 Theory and Practice<br>1.6 Binary Numbers<br><br>**Chapter 2 Introduction to Logic Circuits**<br>2.1 Variables and Functions<br>2.2 Inversion<br>2.3 Truth Tables<br>2.4 Logic Gates and Networks<br>2.5 Boolean Algebra<br>2.6 Synthesis Using AND, OR, and NOT Gates<br>2.7 NANDand NOR Logic Networks<br>2.8 Design Examples<br>2.9 Introduction to CADTools<br>2.10 Introduction to VHDL<br><br>**Chapter 3 Implementation Technology**<br>3.1 Transistor Switches<br>3.2 NMOS Logic Gates<br>3.3 CMOS Logic Gates<br>3.4 Negative Logic System<br>3.5 Standard Chips<br>3.6 Programmable Logic Devices<br>3.7 Custom Chips, Standard Cells, and Gate Arrays<br>3.8 Practical Aspects<br>3.9 Transmission Gates |

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| | 3.10 Implementation Details for SPLDs, CPLDs, and FPGAs<br>**Chapter 4 Optimized Implementation of Logic Functions**<br>4.1 Karnaugh Map<br>4.2 Strategy for Minimization<br>4.3 Minimization of Product-of-Sums Forms<br>4.4 Incompletely Specified Functions<br>4.5 Multiple-Output Circuits<br>4.6 Multilevel Synthesis<br>4.7 Analysis of Multilevel Circuits<br>4.8 Cubical Representation<br>4.9 A Tabular Method for Minimization<br>4.10 A Cubical Technique for Minimization<br>4.11 Practical Considerations<br>4.12 Examples of Circuits Synthesized from VHDL Code<br><br>**Chapter 5 Number Representation and Arithmetic Circuits**<br>5.1 Number Representations in Digital<br>5.2 Addition of Unsigned Numbers<br>5.3 Signed Numbers<br>5.4 Fast<br>5.5 Design of Arithmetic Circuits Using CAD Tools<br>5.6 Multiplication<br>5.9 Examples of Solved Problems Problems<br><br>**Chapter 6 Combinational-Circuit Building Blocks**<br>6.1 Multiplexers<br>6.2 Decoders<br>6.3 Encoders<br>6.4 Code Converters<br>6.5 Arithmetic Comparison Circuits<br>6.6 VHDL for Combinational Circuits<br>6.7 Concluding Remarks<br>6.8 Examples of Solved Problems |

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| 14 | Main reference:<br><br>1. VHDL Programming by Example, Douglas L. Perry, 4th Edition<br>2. Fundamentals of Digital Logic with VHDL Design<br>3. http://www.fpga4students.com |
| 15 | Additional references:<br><br>1. Digital System Design using VHDL,<br>2. http://www.freebookcentre.net/electronics-ebooks-download/VHDL-Language-Guide.html |

**Information on Practical (Digital Design with HDL)**

| Lab | Activity |
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| 1 | **Topic**: **Logic Gates**<br>**Objectives:**<br>i. To apply the logic gate operations<br>ii. To design the VHDL codes for logic gates<br>**Resources**:<br>i. Quartus II Software<br>ii. DE2-115 or DE1 FPGA Education and Development Kit<br>iii. Personal Computer |
| 2 | **Topic**: **Lighting Control System**<br>**Objectives:**<br>i. To design the lighting control system<br>ii. To design of the VHDL codes<br>iii. To analyze the operation of this system with timing diagram<br>**Resources**:<br>i. Quartus II Software<br>ii. DE2-115 or DE1 FPGA Education and Development Kit<br>iii. Personal Computer |
| 3 | **Topic**: **Four Inputs Control System**<br>**Objectives:**<br>i. To design the control system with various inputs<br>ii. To design the VHDL code for this control system<br>iii. To analyze the system operation with timing diagram<br>**Resources**:<br>i. Quartus II Software<br>ii. DE2-115 or DE1 FPGA Education and Development Kit<br>iii. Personal Computer |

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| 4 | **Topic**: **Half Adder**<br><br>**Objectives:**<br>i. To test the operation of half adder logic circuit<br>ii. To design the VHDL code for half adder circuit<br>iii. To analyze the operation of the half adder circuit<br><br>**Resources**:<br>i. Quartus II Software<br>ii. DE2-115 FPGA or DE1 Education and Development Kit<br>iii. Personal Computer |
| 5 | **Topic**: **Full Adder**<br><br>**Objectives:**<br>i. To test the operation of full adder logic circuit<br>ii. To design the VHDL code for full adder circuit<br>iii. To analyze the operation of the full adder circuit<br><br>**Resources**:<br>iv. Quartus II Software<br>v. DE2-115 or DE1 FPGA Education and Development Kit<br>vi. Personal Computer |

Approved By

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